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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|----------------------------------|-------------|----------------------|---------------------|------------------|
| 09/945,247 | 08/31/2001 | Seiichiro Higashi | 9319T-000281 | 1294 |
| 27572 | 7590 | 08/24/2004 | EXAMINER | |
| HARNESS, DICKEY & PIERCE, P.L.C. | | | SOWARD, IDA M | |
| P.O. BOX 828 | | | | |
| BLOOMFIELD HILLS, MI 48303 | | | ART UNIT | PAPER NUMBER |
| | | | 2822 | |

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|------------------------|---------------------|--|
| Office Action Summary | Application No. | Applicant(s) | |
| | 09/945,247 | HIGASHI ET AL. | |
| | Examiner | Art Unit | |
| | Ida M Soward | 2822 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE - MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 02 June 2004.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1.3-5,7,8,10-12 and 14-16 is/are rejected.
- 7) Claim(s) 2,6,9 and 13 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____.

DETAILED ACTION

This Office Action is in response to preliminary amendment filed June 2, 2003.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 5, 7-8, 12 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (5,970,384) in view of Zhang et al. (US 2003/0122131 A1), Grill et al. (US 2002/0037442 A1) and Yamazaki et al. (US 2002/0034863 A1).

In regard to claim 1, Yamazaki et al. (5,970,384) teach a method for the fabrication of a field-effect transistor comprising the steps of: forming a semiconductor layer **704** serving as an active layer on a substrate **701**; forming a stage gate insulating film **705** on the semiconductor layer; heat treating the gate insulating film in an N₂O atmosphere (col. 15, lines 7-37) (Figure 7E, col. 12, lines 40-67).

In regard to claims 5, 8 and 14, Yamazaki et al. (5,970,384) further teach the gate insulating film formed by plasma CVD method using a TEOS gas (col. 5, lines 45-58).

However, Yamazaki et al. (5,970,384) fail to teach an interface level density between the semiconductor layer and the gate insulating film being no less $10^{11} \text{ cm}^{-2}\text{eV}^{-1}$; setting the substrate temperature at no higher than 100°C and heat-treating the gate insulating film in an atmosphere containing water.

In regard to claims 1 and 15-16, Zhang et al. teach the interface level density between the semiconductor layer 204 and the gate insulating film 205 of $10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ or lower which is in the range of no less $10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ (Figures 11(A)-11(B), page 9, paragraph [0093]).

In regard to claims 1, 7 and 15-16, Grill et al. teach setting the substrate temperature at between about 25°C and about 400°C, which is in the range of no higher than or no less than 100°C. (page 2, paragraph [0022]).

In regard to claims 1, 8 and 15, Yamazaki et al. (US 2002/0034863 A1) teach heat-treating in an atmosphere containing water after the formation of a first-stage gate insulating film (page 13, paragraph [0269]).

Since Yamazaki et al. (5,970,384), Zhang et al., Grill et al. and Yamazaki et al. (US 2002/0034863 A1) are from the same field of endeavor (method of manufacturing semiconductors), the purpose disclosed by Yamazaki et al. (US 2002/0034863 A1) would have been recognized in the pertinent art of Yamazaki et al. (5,970,384), Zhang et al. and Grill et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method for the fabrication of a field-effect transistor of Yamazaki et al. (5,970,384) with the interface level density of Zhang et al.; the substrate temperature of Grill et al. and the atmosphere containing

water of Yamazaki et al. (US 2002/0034863 A1) to obtain a semiconductor device having an excellent performance (page 13, paragraphs [0269]-[0273]).

Claims 3-4 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. (5,970,384), Zhang et al. (US 2003/0122131 A1), Grill et al. (US 2002/0037442 A1) and Yamazaki et al. (US 2002/0034863 A1) as applied to claims 1, 5, 7-8, 12 and 14-16 above, and further in view of An et al. (US 6,245,618 B1).

Yamazaki et al. (5,970,384), Zhang et al., Grill et al. and Yamazaki et al. (US 2002/0034863 A1) teach all mentioned in the rejection above. However, Yamazaki et al. (5,970,384), Zhang et al., Grill et al. and Yamazaki et al. (US 2002/0034863 A1) fail to teach conducting a process while cooling a substrate.

An et al. teach conducting a process while cooling a substrate (col. 1, lines 46-56).

Since Yamazaki et al. (5,970,384), Zhang et al. Grill et al., Yamazaki et al. (US 2002/0034863 A1) and An et al. are from the same field of endeavor (method of manufacturing semiconductors), the purpose disclosed by An et al. would have been recognized in the pertinent art of Yamazaki et al. (5,970,384), Zhang et al. Grill et al. and Yamazaki et al. (US 2002/0034863 A1). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method for the fabrication of a field-effect transistor of Yamazaki et al. (5,970,384), the interface level density of Zhang et al., the substrate temperature of Grill et al. and the

atmosphere containing water of Yamazaki et al. (US 2002/0034863 A1) by incorporating cooling a substrate of An et al. to reduce junction leakage current (col. 1, lines 46-56).

Allowable Subject Matter

Claims 2, 6, 9 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respects to a method for fabricating field effect transistors:

Suguro (US 2004/0070045 A1)

Zhang et al. (5,424,244).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M Soward whose telephone number is 571-272-

1845. The examiner can normally be reached on Monday - Thursday, 6:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
August 5, 2004



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